ITT
Semiconductors

VMOS Application Ideas

compiled by the following members
of the ITT Semiconductors Group

Leslie Miskin, B. Sc., Freiburg
Günter Peltz, Eng., Freiburg
Richard Pickvance, B. A., Footscray
Hermann Dieringer, Eng., Freiburg

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Preface

This should be read as an *ideas book*. It is intended to stimulate the reader's creativity. The circuits showing no component values are suggestions, which the reader should adapt to his practical requirements.

Introduction

1. Introduction

1.1. General

Normal MOS field effect transistors (MOS FETs) are known for their high ON resistance and unfavourable switching characteristics. The reason for these lies in the relatively imprecise structure that a lateral transistor has. The channel length, upon which the ON resistance depends, cannot be less than a certain amount. The necessary overlapping of the gate electrode over the drain and source leads to a high capacitance which means long switching times and a low cutoff frequency. Transistors using this MOS FET technology cannot be made for high frequencies.

If instead of using the lateral structure (Fig. 1b), whose precision depends upon masking, a vertical VMOS structure is employed, then it is smaller in area and its precision depends upon diffusion depth (Fig. 1a). The channel length is that of the extremely thin "body" of the transistor and this produces a very low ON resistance. The capacitance is lower because the overlap is very much less. VMOS technology thus permits an MOS transistor to be improved by conferring on it a low ON resistance and very good H. F. properties, while retaining the extremely high input resistance and low H. F. noise.

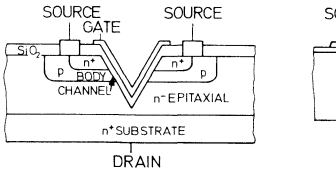


Fig. 1: Technology: a) VMOS structure b) Lateral MOS FET

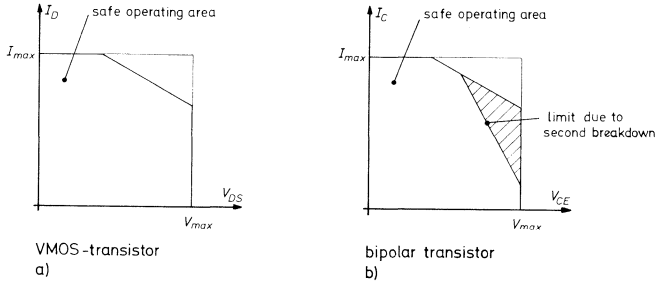
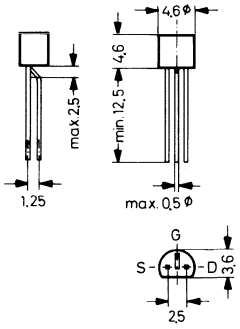
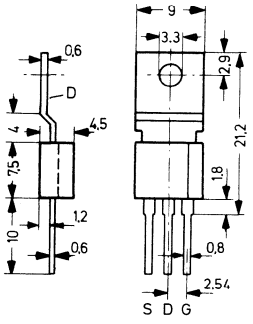


Fig. 2: Safe operating area for a) VMOS transistors b) Bipolar transistors



Plastic Case of Types BS107, BS170, BS250



Plastic Case of Types BD512, BD522

N-Channel VMOS Transistors

Type	Absolute Maximum Ratings			Characteristics at T_j = 25 °C							
	Drain-Source Voltage	Drain Current (continuous)	Power Dissipation at T_C = 25 °C	Gate Threshold Voltage at $V_{GS} = V_{DS}$, I_D = 1 mA	Drain-Source ON Resistance[1] at V_{GS} = 10 V, I_D = 0.2 A	ON Resistance[1] at V_{GS} = 10 V, I_D = 1 A	ON Resistance[1] at V_{GS} = 2.6 V I_D = 20 mA	Drain Cutoff Current at V_{DS} = 25 V, V_{GS} = 0	Drain Cutoff Current at V_{DS} = 130 V, V_{GS} = 0	Forward Transconductance[1] at V_{DS} = 10 V, I_D = 0.2 A	Forward Transconductance[1] at V_{DS} = 10 V, I_D = 0.5 A
	V_{DSS} V	I_D A	P_{tot} W	$V_{GS\,(th)}$ V	$r_{DS\,(ON)}$ Ω	$r_{DS\,(ON)}$ Ω	$r_{DS\,(ON)}$ Ω	I_{DSS} μA	I_{DSS} nA	g_m mS	g_m mS
BS107	200	0.12	0.5	–	–	–	15 (< 28)	–	< 30	–	–
BS170	60	0.5	0.83	0.8 . . . 3	3.5 (< 5)	–	–	< 0.5	–	200	–
BS522	60	1.5	10	0.8 . . . 3	–	2 (< 3)	–	< 0.5	–	–	400

[1] Pulse Test Width – 80 μs, Pulse Duty Factor 1%

P-Channel VMOS Transistors

Type	Absolute Maximum Ratings			Characteristics at T_j = 25 °C					
	Drain-Source Voltage	Drain Current (continuous)	Power Dissipation at T_C = 25 °C	Gate Threshold Voltage at $V_{GS} = V_{DS}$, $-I_D$ = 1 mA	Drain-Source ON Resistance[1] at $-V_{GS}$ = 10 V, $-I_D$ = 0.2 A	ON Resistance[1] at $-V_{GS}$ = 10 V, $-I_D$ = 1 A	Drain Cutoff Current at $-V_{DS}$ = 25 V, V_{GS} = 0	Forward Transconductance[1] at V_{DS} = 10 V, $-I_D$ = 0.2 A	Forward Transconductance[1] at $-V_{DS}$ = 10 V, $-I_D$ = 0.5 A
	$-V_{DSS}$ V	$-I_D$ A	P_{tot} W	$-V_{GS\,(TO)}$ V	$r_{DS\,(ON)}$ Ω	$r_{DS\,(ON)}$ Ω	$-I_{DSS}$ μA	g_m mS	g_m mS
BS250	45	0.5	0.83	1.0 . . . 3.5	9 (< 14)	–	< 0.5	150	–
BD512	60	1.5	10	1.0 . . . 3.5	–	4.5 (< 7)	< 0.5	–	300

[1] Pulse Test Width – 80 μs, Pulse Duty Factor 1%

Besides this, VMOS transistors are more tolerant of overloads: there is no forward second breakdown (Fig. 2) and the ON resistance has a positive temperature coefficient. This means that the drain current becomes less as the temperature of the transistor increases, so making the transistor self-protective. Furthermore this makes paralleling of transistors easy because there is no current hogging. Table 1 compares VMOS and bipolar transistors.

Table 1:
Main parameters of bipolar and VMOS transistors

Parameter	Bipolar	VMOS
Input resistance	$10^3...10^5\ \Omega$	$10^9...10^{11}\ \Omega$
Power amplification	100...200	$10^5...10^6$
Switch-on time	50...500 ns	4 ns
Switch-off time	500...2000 ns	4 ns
ON resistance	0.3 Ω	3 Ω
Breakdown characteristics	bad, second breakdown	good
Parallel operation	only with special circuits	no difficulty

1.2. Complementary VMOS devices

As the mobility of electrons is double that of holes, P-channel VMOS devices have about double the ON resistance of N-channel devices for the same chip area. Other characteristics of the P-channel types are not necessarily scaled by the same factor.

1.3. Drain-source diode

In every VMOS device there is inherently a diode connected between source and drain. In the N-channel device the anode of the diode is formed by the body layer, while the n^+ and n^- layers of the drain form the cathode. The characteristics of the diode are not specified on the data sheets as it is not intended to be used. However, the diode on the n-channel devices is a "good" diode quite similar to a conventional diode of 0.5 to 1 A rating. The diode on the P-channel devices shows a drop of several volts at comparable currents.

1.4. Handling

VMOS devices without gate protection diodes must be handled like MOS integrated circuits, i. e. with due precautions to avoid build-up of charge on the gates.

Although the positive temperature coefficient of the channel resistance of VMOS devices helps to make them thermally stable, it is still necessary to provide adequate heatsinking. Testing VMOS devices on a curve tracer can be dangerous because of their high f_T and because of the high instantaneous powers that can be applied by such equipment.

2. Power supply

For linear regulators, VMOS devices offer good high frequency performance, very low drive requirements, and no saturation voltage. In switching power supplies VMOS devices are outstanding performers: their fast switching capability makes feasible power conversion at megahertz rates, with consequent size reduction. At these higher frequencies switch-mode power supplies can also respond to changes of line or load conditions just as quickly as conventional linear regulators. Power densities of over 5 W/cm^3 are attainable.

2.1. Linear regulators

Fig. 3 shows how to exploit the absence of saturation voltage. With conventional regulators the minimum input-output voltage differential is limited by the saturation voltage of the series pass transistor. To obtain a really low saturation voltage requires heavy base drive. With VMOS the ON characteristic is purely resistive: the input-output differential depends only on the product of the load current and this resistance. Furthermore, the drive current requirements are negligible, so that the control signal can be provided by even a low-power operational amplifier.

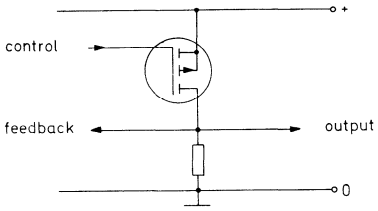


Fig. 3: Linear regulator

2.2. Switch-mode d.c. to d.c. conversion

The simplest types of non-isolating regulators are shown in Figs. 4, 5 and 6. In practical circuits the operating frequency is limited more by the surrounding components than by the VMOS devices themselves. Electrolytic capacitors designed for switch-mode applications should be used, or non-electrolytic capacitors (polycarbonate, polypropylene, etc.) for the higher frequencies.

The step-up circuit of Fig. 4 can be developed as shown in Fig. 7 as a simple inverter for fluorescent lamps. The circuit can be used with a fixed duty cycle in the switch. By adding the current-sensing network RC a regulating circuit can be created which is independent of supply voltage variations. Of course, a fully adjustable dimmer circuit is made by varying the duty cycle either with or without the aid of feedback. The transformer secondary voltage overshoots as far as is necessary to cause the fluorescent lamp to strike. The

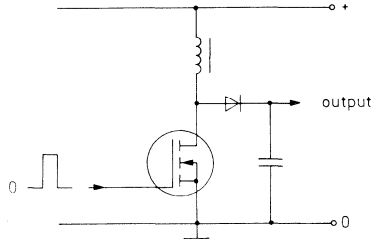


Fig. 4: Step-up circuit

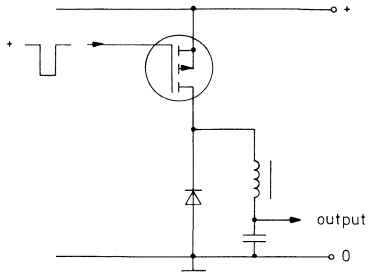


Fig. 5:
Step-down circuit

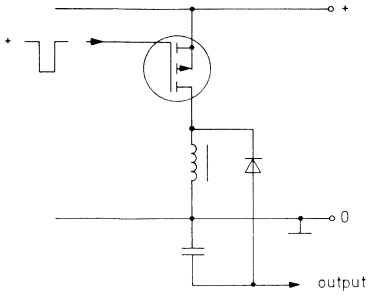


Fig. 6:
Polarity inverter

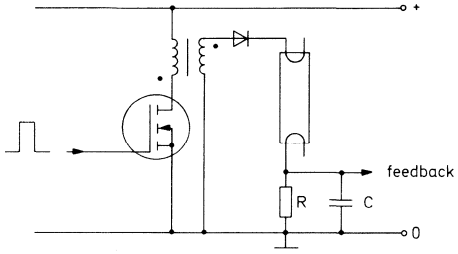


Fig. 7:
Fluorescent lamp drive

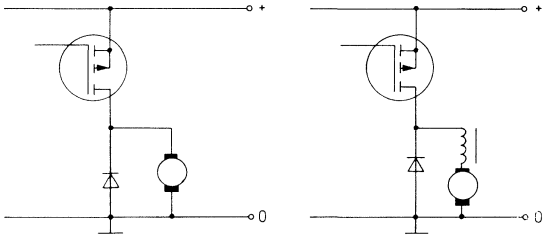


Fig. 8: Speed control of small d.c. motors
a) Motor inductance as filter
b) Low inductance motor with external filter

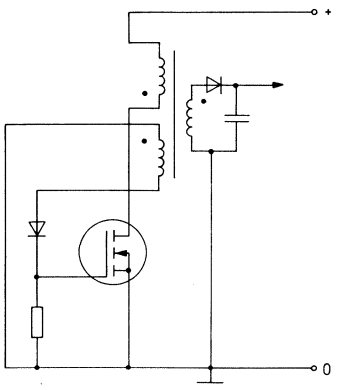


Fig. 9:
Converter circuit with blocking oscillator

transient voltage conditions on the VMOS device should therefore be analysed carefully, with particular attention to leakage inductance in the transformer (ref. 1). Depending on the ratio of the positive voltage to the negative on the transformer secondary, the diode shown will not always be required.

The step-down regulator circuit of Fig. 5 can be used for controlling the speed of d.c. motors as shown in Fig. 8. The inductance of the motor itself is used as the filter element in Fig. 8a. Some types of motor, e.g. "printed circuit" motors and other motors with ironless rotors, can have very low inductance ($< 100\ \mu H$): for these some additional external inductance as shown in Fig. 8b is advisable unless a very high switching frequency is used.

A selection of d.c. to d.c. converter circuits is shown in Figs. 9 to 11. These are all circuits that were used with bipolar transistors. Fig. 9 is the familiar blocking oscillator. Fig. 10 is a voltage-feedback converter using a saturating transformer. (The factors that make current-feedback converter circuits

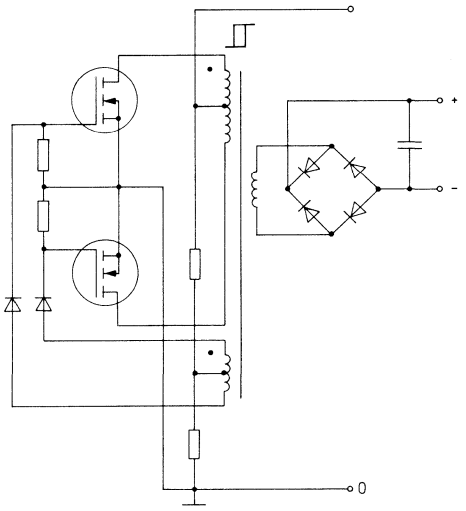


Fig. 10: Voltage-feedback converter

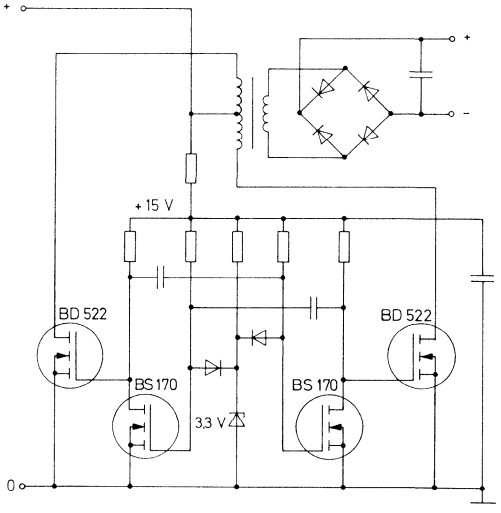


Fig. 11: Multivibrator-driven converter

attractive for bipolar transistors are largely inapplicable to VMOS.) Two-transformer converters are also possible. Fig. 11 shows a simple driven converter in which the drive waveforms come from a multivibrator. The multivibrator can be built with bipolar transistors or, as shown, with VMOS transistors for the ultimate in speed. Resistors on the gates of the VMOS devices must be dimensioned to avoid slow rise and fall times due to gate capacitance. Besides these circuits, many other converter circuits using transistors or squarewave inverters using SCRs can be redesigned to use VMOS. Many of the sinewave inverters in section 2.4. below can of course be used for d.c. to d.c. conversion. Circuits using both VMOS and bipolar power transistors for d.c. to d.c. conversion are given in ref. 2.

2.3. Voltage doubler power supply

Perhaps this name is too optimistic because there are losses and the voltage is not twice the original circuit. The VMOS transistors can be driven by a CMOS logic circuit which is oscillating at a high frequency: 50 kHz was used but the frequency can be much higher.

To understand the circuit Fig. 12a, suppose T1 is switched on by the gate voltage of V_S; T2 will hence be switched off. C1 will charge to $V_S - V_{f(D1)}$ because the drain of T1 is virtually at 0 volts. When the drive voltage goes to zero, T1 is switched off quickly (there is no storage time because it is a majority carrier device) and T2 is switched on. This connects the bottom end of C1 to V_S and the other end of C1 will be at $V_S + (V_S - V_{F(D1)})$ which is approaching twice the supply voltage. D1 is now reverse biased and C1 will tip its charge into C2 via D2, which is now forward biased. The voltage on C2 will rise and the final voltage depends upon the time constants of the circuit. The cycle is then repeated and the voltage across C2 will eventually rise to $2V_S - 2V_F$ if there is no current flowing through the load.

The voltage ratings of T1, T2 and C1 must be greater than or equal to V_S and for C2 should be $2V_S$. The VMOS transistors have a certain ON resistance which limits initial current flow to a safe amount. If high outputs are needed, the transistors BD 512 and BD 522 can be directly bolted onto the same heat sink because their drains are connected together and the drains are bonded to the tabs. For low currents the BS 170 and BS 250 can be used.

Table 3:

Output characteristics of Fig. 12a, using BD 512/BD 522

V_S	V_{out}	I_{Load}	Efficiency
10 V	16.4 V	82 mA	72 %
10 V	17.8 V	18 mA	62 %

Fig. 12b shows a variant of the circuit Fig. 12a, having a supply voltage higher than the gate-source voltage of the VMOS transistors. Due to clamping by means of diodes, the required driving signal is available at the gates. The dashed diodes are really necessary only in the case of VMOS devices without integrated Zener protection diodes. In the case of a driving signal having short rise and fall times, which is useful for small power dissipation in the VMOS transistors, these diodes should be of the Schottky type, e.g. SD 101 of ITT.

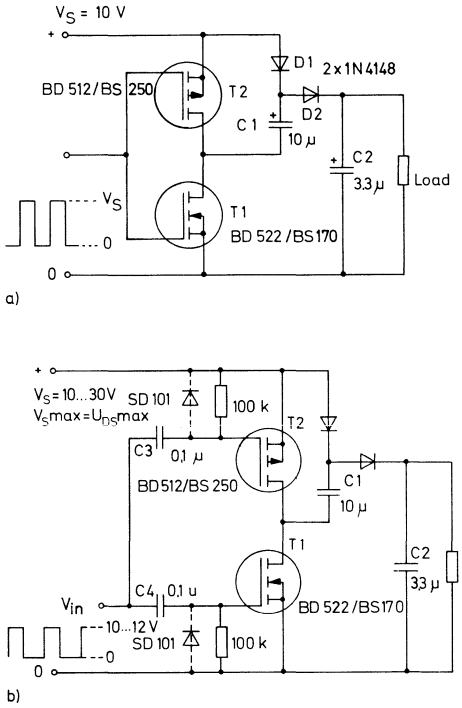


Fig. 12: Voltage doubler power supplies
a) for low supply voltage
b) for high supply voltage

2.4. Sinewave inverters and oscillators

The Figs. 13 to 17 give a selection of sinewave inverter circuits, most of which originally used SCRs. The drive waveforms required can be obtained from integrated circuits designed for push-pull power converters. Supplying drive to the VMOS is particularly simple if devices of both polarities are used: if all devices are of one polarity, as with SCRs, pulse transformers are required.

The calculation of component values for these types of inverter is complicated by the large number of variables. The peak/ d.c. ratios of currents and voltages can be controlled by suitable design, e.g. by adjustment of the ratio L2/L1 and the ratio of the drive frequency to the natural resonant frequency of the circuit.

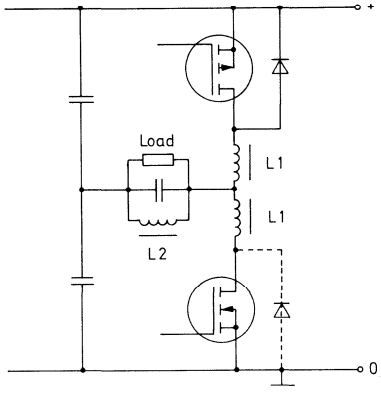


Fig. 13: Sinewave inverter, capacitive half-bridge

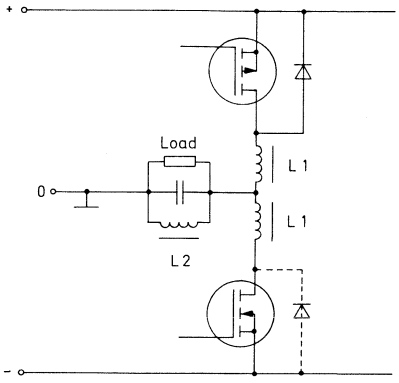


Fig. 14:
Sinewave inverter, center-tapped half-bridge

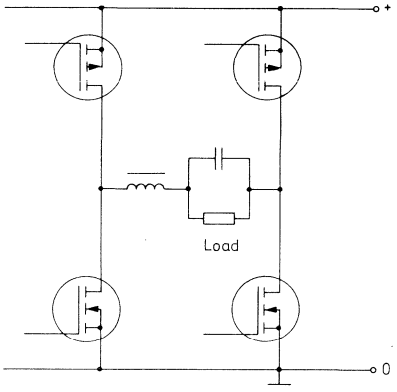


Fig. 15:
Sinewave inverter, full bridge 1

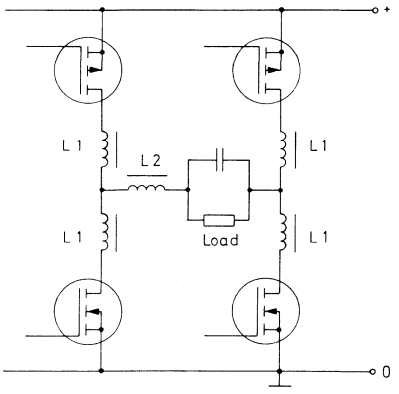


Fig. 16:
Sinewave inverter full bridge 2

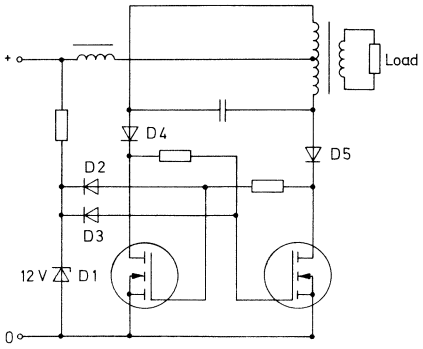


Fig. 17:
Tuned self-oscillating sinewave inverter

The circuit of Fig. 17 shows a Zener diode D1 used to limit the gate drive voltages. The small-signal diodes D2 and D3 prevent the Zener diode capacitance from appearing in parallel with the gate capacitance. The waveforms at the drains of the VMOS devices are half-sinusoids with peak amplitudes of $\pi \cdot V_S$. There are also variants of this circuit in which the series diodes D4 and D5 are not used.

Fig. 18 shows how an SCR circuit can be converted to VMOS. Fig. 18a is the basic circuit. Fig. 18b shows the drive voltage being obtained from a simple bistable. The input pulse is of uncritical duration. Fig. 18c shows the current passing through L1 or through the VMOS transistor/parallel diode combination, for a single cycle of operation starting when the circuit is triggered by the input pulse. When the current reverses and starts to flow through the diode, the diodes D1, D2 reset the bistable. The time at which this resetting occurs is not critical provided that it occurs well before the end of the period t_d.

If the input pulse shape can be accurately defined the simpler circuit of Fig. 18d becomes feasible. When SCRs were used in this circuit the period t_d, being the available time for the SCR to turn off, could not be allowed to fall too low. With VMOS this restriction is much less significant: speed limitations have more to do with gate capacitance and the source impedance that feeds it.

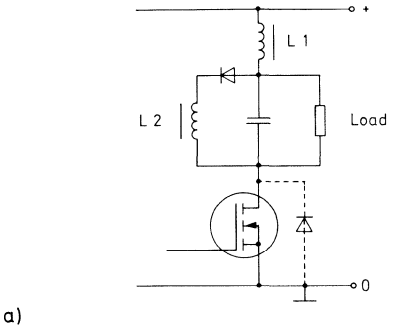
Apart from the circuits illustrated here other conventional linear oscillators can be built, but their efficiencies will of course be lower than those of switch-mode sinewave inverters. The Class E output stage (section 4.2.) can also be treated as a high power sinewave inverter.

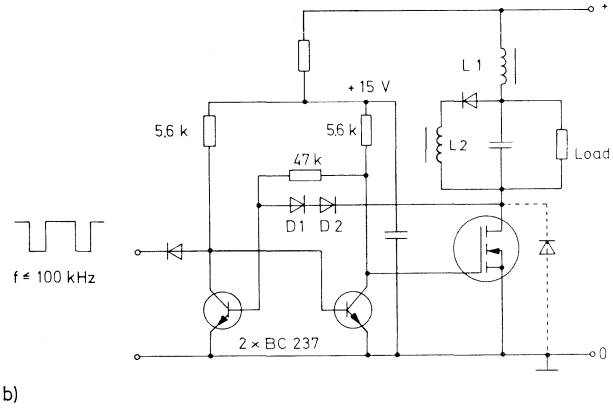
Inverters and oscillators like these find application in battery-powered fluorescent lighting, in bias and erase oscillators for tape recorders and for driving ultrasonic transducers, particularly piezoelectric ceramic discs or rings. In fluorescent lighting the high operating frequencies that are feasible with VMOS result in much smaller ballast chokes, wound on ferrite with resultant savings of size and cost. Typical high-power ultrasonic applications include cleaning (20...50 kHz), atomisation (> 1 MHz), welding and soldering.

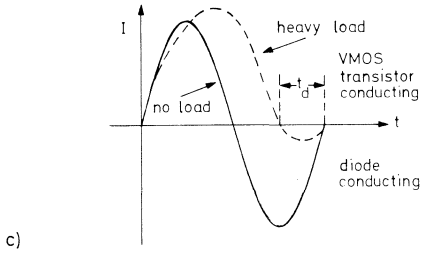
2.5. Current sources

Because of their high output impedances, VMOS devices make good current sources even when unregulated. Figs. 19a and 19b show uncompensated and temperature-compensated sources of this kind. In Fig. 20 the regulated current source suffers from the temperature coefficient of the base voltage of the bipolar transistor.

The Fig. 21 circuit relies on the equality of source and drain currents for its accuracy. When bipolar transistors are used in the same circuit the base current introduces an error, whereas the extremely low gate current of VMOS devices, particularly the BS 170 and BS 250, avoids the error, even when the sourced current is at the milliampere level. Useful two-terminal high-current sources can be made with the circuit of Fig. 19c if the resistor values are kept very high.







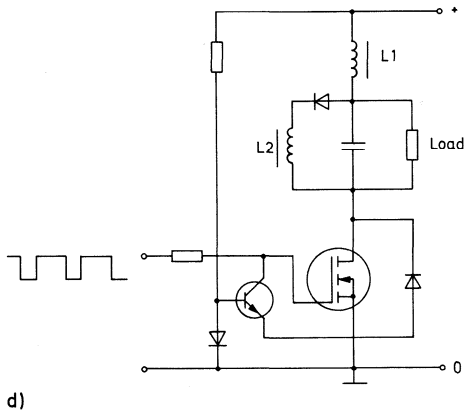


Fig. 18: Conversion of a circuit for SCR to VMOS
a) Basic circuit
b) Bistable driver
c) Current in circuit
d) Simplest circuit

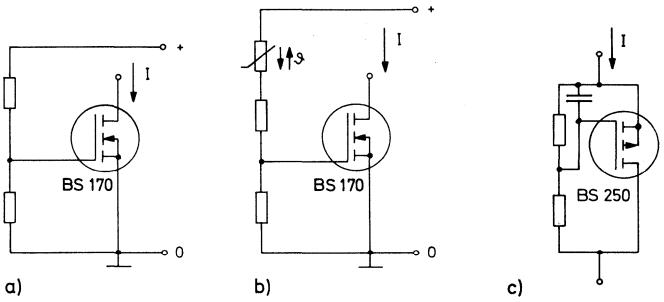


Fig. 19: Unregulated current sources
a) No temperature compensation
b) Temperature compensated
c) Two-terminal current source

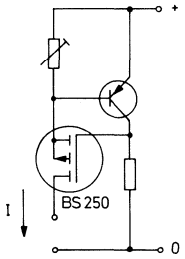


Fig. 20: Regulated current source

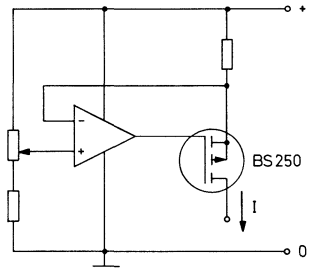


Fig. 21: Regulated temperature-independent current source

2.6. Three-phase motor drive

Fig. 22 shows a basic three-phase voltage drive circuit where the outputs are squarewaves at one-sixth of the input frequency. The VMOS devices can be driven directly by the 4018 CMOS presettable divider if the IC and the VMOS transistors are powered by the same 10...15 V supply. For higher output power and higher supply voltage the use of coupling capacitors as shown in Fig. 12b can be useful.

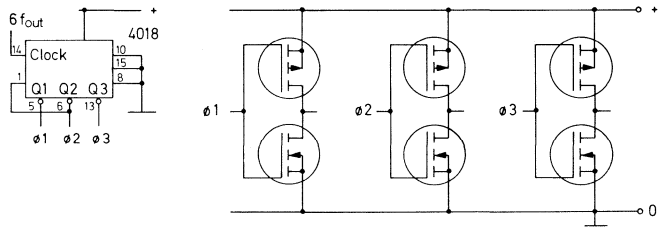


Fig. 22: Three-phase motor drive, basic circuit

Low frequency amplification

Figs. 23 and 24 indicate how a gating waveform G or $\overline{G}$ can be added to the basic drive circuit so that the output can be pulse-width modulated. This is based on a suggestion by Heinrich Backhausen, Krummstr. 16, D-4048 Grevenbroich 2, relating to driving an immersion (poker) vibrator used in placing concrete. In this application the pulse-width modulation is used as a power output control, and up to 55 V r.m.s. at 200...600 Hz is obtained from a 60 V rail.

In such circuits, pulse-width modulation at high frequencies can also be used to synthesize a waveform at lower frequencies. This is equivalent to the cycloinverter circuits used with SCRs.

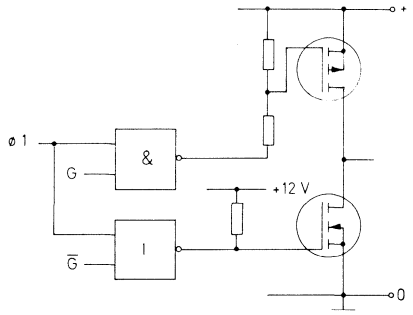


Fig. 23: Gating the output stages of Fig. 22

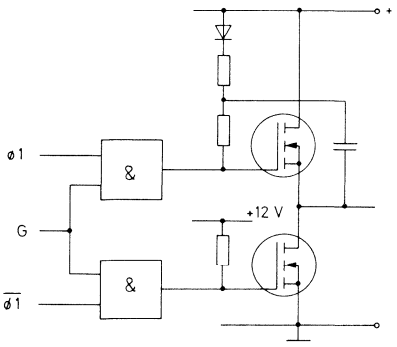


Fig. 24. Gating non complementary output stages

3. Low frequency amplification

For linear amplifiers VMOS devices offer excellent high frequency performance (f_T > 400 MHz) and linearity. At currents over about 0.2 A the transconductance of the BD 512 and BD 522 is independent of current. For switch-mode amplification the advantages of VMOS transistors in switch-mode power supplies are equally relevant.

3.1. Class A amplifiers

The basic Class A amplifier stage of Fig. 25 can operate with high-value bias resistors (R1 and R2). Together with the high output impedance of the VMOS device this means that the cascaded stage gain may be taken simply as $g_m \cdot R_L$. In practice stage gains of over 30 dB are obtainable and this gain extends into the megahertz region. A resistor may be included in series with the source, not for the sake of thermal stability (as this is already satisfactory) but to reduce the spread of performance of the circuit.

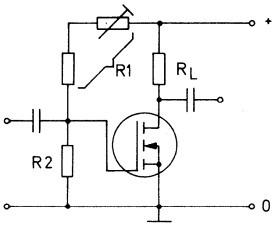


Fig. 25: Basic Class A amplifier stage

Another solution for eliminating the influence of the gate threshold voltage production spread is shown in Fig. 26. The bias of the VMOS transistor is stabilized by means of negative voltage feedback running from drain to gate.

Fig. 27 shows an application as an ultrasonic transmitter driver for TV remote control. The resistor network on the gate of the VMOS transistor defines the peak current into the coil. For tighter performance spreads a source resistor may be added.

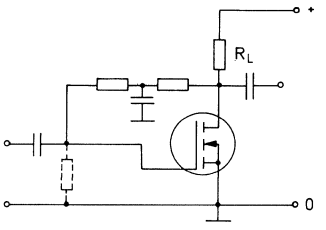


Fig. 26: Class A amplifier with voltage feedback

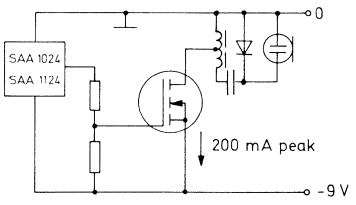


Fig. 27: Ultrasonic transmitter driver

3.2. Class ABC amplifier with complementary VMOS transistors

The title is not a printing error. Although it is basically a Class B amplifier, one of the transistors is more in Class A, while the other is definitely in Class C. There are Class AB amplifiers, so why not Class ABC as well. The circuit Fig. 28 was designed for modest requirements, and because of the paucity of components, the distortion is not very small.

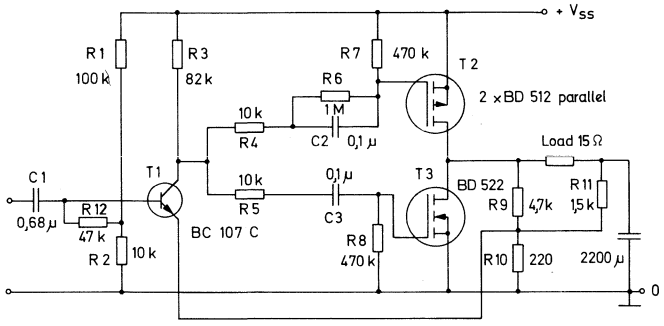


Fig. 28: Complementary Class ABC amplifier

A fairly unusual feature is that a common-source configuration is used. An advantage of such a circuit is that there is voltage amplification so that the drive does not have to exceed the supply voltage. Two other advantages of VMOS transistors are that the power gain is almost infinite, and that output power can be increased by paralleling transistors without altering the drive circuit; attempting to do this with bipolar output transistors would lead to disaster, but VMOS transistors think nothing of it. Yet another, but not so obvious, bonus is that the drains of the VMOS transistors are electrically connected. In a VMOS transistor in a TO-202 package, the drain is connected to the tab: thus both the tabs can be directly bolted to the same heat sink without needing insulating washers.

P-channel VMOS transistors are only half as good as N-channel as regards ON resistance and g_m: this is because holes (the majority carriers of P-channels) are half as fast as the electrons of the N-channels. This means that twice as many P-channel transistors should be used as N-channel transistors, to compensate for the difference. The threshold voltage of VMOS transistors is determined by manufacture, not by semiconductor physics, and is hence not a fixed quantity. This means that only an approximate bias is given, and negative feedback has to compensate for these variations.

The first stage of the circuit Fig. 28 operates at low current and high gain, which also helps the noise figure to be low. The input impedance can be seen to be about 50 kΩ but it can be increased by increasing the 47 kΩ resistor. T1 is a common emitter bipolar transistor with emitter feedback. Its collector is connected in a somewhat peculiar way to the gate of T2 (actually T2 is two BD 512 in parallel). C2 is to by-pass R6, otherwise only a very small signal would appear on the gate of T2. R4 and R5 are there only to stop oscillations. The same alternating voltage is applied to the gate of T3 via capacitor C3. A question at this point is "where is the bias for T3?" Obviously it will distort without a bias to bring it up to its threshold, but this is taken care of by the a.c. negative feedback. A subsidiary question would be "why is d.c. bias applied to T2 only?": the reason is that at least one transistor must conduct to define the d.c. quiescent point of the output to keep it to half the supply voltage. It would be very pleasing to bias T3, but this would be complicated and it would involve a constant current source; this would be expensive.

The load is connected in a somewhat unusual way, but it can be seen that an a.c. plus d.c. signal is present at the 2200 µF electrolytic output capacitor. Thus a.c. and d.c. feedback is applied to T1 via R9 and R10, but a heavier d.c. feedback is applied via R11 and R10 to stabilize the quiescent d.c. voltage to half V_{SS} and it can be seen from one of the graphs that this is quite successful. A further improvement to the circuit would be to replace T1 by a small VMOS transistor. The noise would probably be less and biasing resistors having considerably higher values could be used, thus matching the circuit to very high impedance transducers.

The voltage gain of the circuit Fig. 28 is 30, and the bandwidth amounts to 35 Hz – 125 kHz (at –6 dB), but there is increased distortion above 25 kHz. The Figs. 29a–e demonstrate the circuit performance.

3.3. Class D amplifiers

3.3.1. Basic characteristics

The basic principle of a practical Class D output stage is shown in Fig. 30. The two switches are closed alternately at a high frequency f_s to produce in R_L a waveform whose duty cycle is averaged out (by the inductor) to give a required low-frequency waveform f_m. The drive waveform for the switches has only two states and is normally derived from a comparator which is in turn fed by a composite waveform consisting of the desired audio waveform superimposed on a triangular wave at the switching frequency. It is the instantaneous value of this composite waveform that, when compared with a suitable fixed reference voltage by the comparator, creates the varying duty cycle of the drive waveform for the output stage. Other arrangements are possible to achieve the same effect. The following characteristics of Class D operation are fundamental:

1) Assuming that the switch elements consist of a perfect switch in series with a finite resistance R_{ON}, as shown in Fig. 30 – an assumption that is true for VMOS devices – and further assuming that the inductor is lossless, the efficiency η of the output stage is given by

$$\eta = R_L/(R_L + R_{ON})$$

and tends to 100 % as R_{ON} reduces to zero. Thus efficiency is independent of the audio output level.

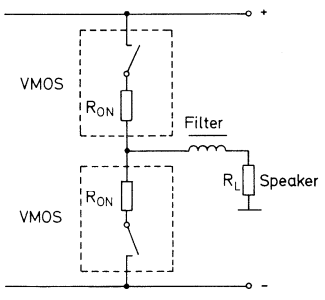
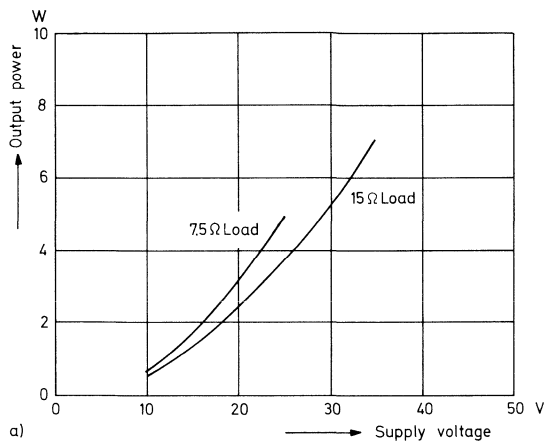
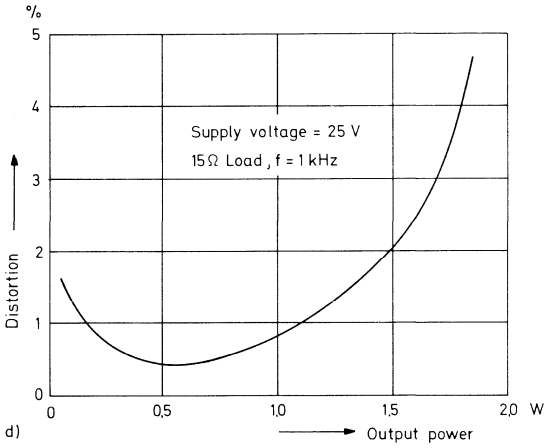
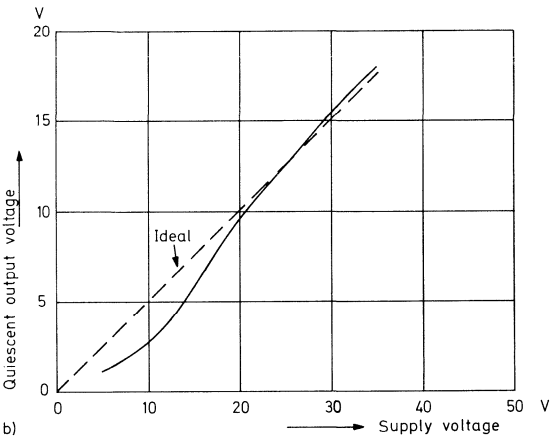
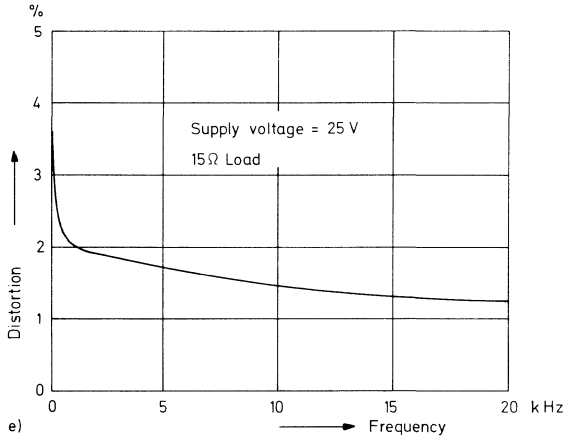


Fig. 30: Basic principle of VMOS Class D amplifier









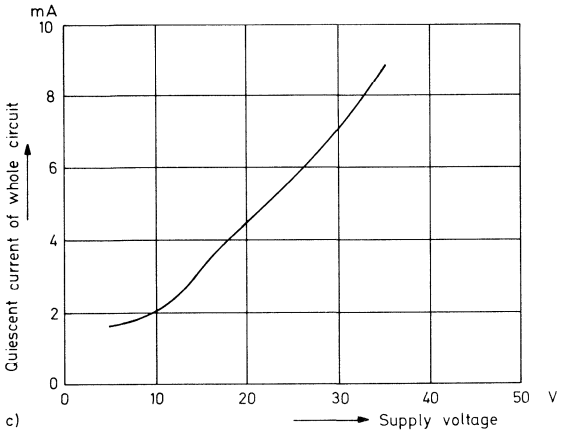


Fig. 29: Results of circuit Fig. 28
a) Output power vs. supply voltage
b) Quiescent output voltage vs. supply voltage
c) Quiescent current (whole circuit) vs. supply voltage
d) Distortion vs. output power
e) Distortion vs. frequency

2) Class D amplifiers are normally based on pulse-width (= pulse ratio) modulation rather than any other type of modulation. The modulation index M is

$$M = \left| \frac{t_{on} - t_{off}}{t_{on} + t_{off}} \right|$$

where t_{on} and t_{off} are respectively the on time and the off time of the switch elements. It will be seen that the efficiency of the output stage is independent of M. This is another way of saying what is in the preceding section, but it means that for a given power supply voltage the penalty of not modulating fully is to reduce the maximum power output but not to reduce the efficiency.

3) In practical switch elements very high instantaneous power losses occur at the on/off transitions. When averaged over a complete switching cycle, the loss of power in this way may (depending on switching frequency) cause a significant degradation of the theoretical efficiency.

4) In practical circuits the amplitude of the triangle waveform is kept constant, whereas the power supply voltage to the output stage may carry ripple or be subject to line regulation. The open-loop gain of a practical Class D system thus varies directly with the supply voltage to the output stage.

5) It follows from the preceding section that any ripple or noise present on the power supply of the output stage is fed directly to the load, unless reduced either by feed-forward compensation or by negative feedback.

6) The amplitude of the switching waveform is very large. Even after filtering (see below) it may still be high enough to cause radiated interference.

7) As with any switching type circuit, if the switch elements have a positive temperature coefficient of resistance there can be a sort of "thermal runaway" effect. The switch elements must therefore be provided with adequate designed heat sinks (however small) so that the equilibrium temperature reached in the elements is within safe limits.

3.3.2. VMOS devices for Class D

VMOS transistors have several characteristics that make them particularly suitable for Class D usage:

1) The absence of an offset voltage means that efficiency can be increased asymptotically by paralleling devices as desired.

2) The fast switching speeds allow a high ratio of switching frequency f_s to modulation (audio) frequency f_m, as is required for low distortion and easy filtering (see below).

3) The symmetrical switching times allow a high modulation index even at high switching frequencies, so giving the maximum power output for any supply voltage.

4) The fast switching times and, in particular, the absence of a "saturation time" mean that turn-on and turn-off behaviour are closely controlled by the gate waveform. This can avoid the need for catching diodes in the output stage (see below).

All in all, VMOS devices are the first active devices adequate to make Class D audio amplifiers practical. Bedford's patent filed in 1930 (ref. 3) used thyratrons!

3.3.3. Modulation and the Class problem

Taking Fig. 30 as a starting point, there are still many ways of driving the switches. The type of modulation where one or other of the output devices is always conducting is defined as Class AD. If only one of the switches is turned on during the positive half cycle of the audio signal, and only the other switch during the negative half cycle, this is called Class BD.

A compromise Class ABD is also possible (ref. 4). During the dead time when neither device is conducting the current in the inductor which is the input element of the filter is returned to the appropriate power rail by a catching diode. The need for these diodes causes two problems. Firstly, it leads to a form of distortion similar to the crossover distortion which is characteristic of Class B output stages. Secondly, there are no diodes available that are suitable for the duty. The only diodes faster than VMOS are Schottky diodes, and these suffer from limited breakdown voltages and capacitances that are high enough to affect the operation of the VMOS. The next fastest diodes are large epitaxial types, which can only be used if the switching edges of the VMOS devices are deliberately slowed down, and this is clearly nonsensical, as it must reduce efficiency. Class AD operation is therefore assumed in the remaining discussion.

3.3.4. Distortion

Pulse-width modulation generates a large spectrum of cross-modulation products including $f_s \pm f_m$, $f_s \pm 2f_m$, etc. The higher order terms are of lower amplitudes, and the relative amplitudes of all the cross-modulation products vary with the modulation index. In practice the only products that are important are those falling between f_m and f_s, because some of them must come within the audio band and can be heard if their amplitudes are sufficient. Cross-modulation products are not harmonically related to f_m and therefore are subjectively less acceptable than equivalent amounts of harmonic distortion. For this reason a minimum ratio of 5, and preferably 10, is recommended between f_s and the upper limit of the audio band in hi-fi applications. With VMOS devices such switching frequencies are quite feasible, and the optimum value of f_s is probably around 500 kHz.

Besides cross-modulation distortion, distortion arises in Class D amplifiers from non-linearity in the modulation process, i.e. in practice, from non-linearity in the triangle wave. Pulse-width modulation for Class D amplification can perfectly well use a sawtooth waveform in place of the triangle, but the resulting cross-modulation products are of higher amplitudes. Thus non-linearity on the slopes of the triangle wave results in harmonic distortion, but asymmetry results in increased cross-modulation distortion.

Any operational amplifier or comparator used for the integrator must have adequate slew rate.

3.3.5. Filters

The filter at the output af a Class D amplifier must consist, at the very least, of an inductor as shown in Fig. 30. The inductance of the loudspeaker itself must not be relied upon for this purpose, nor to present a defined impedance to load the filter. In the circuits of Fig. 31 the filter is terminated by R_M

which is brought into circuit by C_M. The value of C_M needs to be selected according to the impedance of the loudspeaker around the cut-off frequency of the filter, but is not necessarily critical. The value of R_M may differ from the nominal impedance of the loudspeaker.

In order to reduce the amplitude of the switching frequency at the output terminals of the system to a reasonable level, either a filter of gentle slope and low turnover frequency or a filter with a steep slope and higher turnover frequency may be used. There is something to be said for either choice. For the second solution advantages include smaller component values and a smaller group delay. If the turnover frequency is set high, e.g. at the geometric mean of f_s and the highest audio frequency – or slightly higher – the audio band falls entirely within the linear-phase region of the filter even if it is a sharp cut-off type. Filters may be calculated as shown in the references 1, 5, 6 and 7.

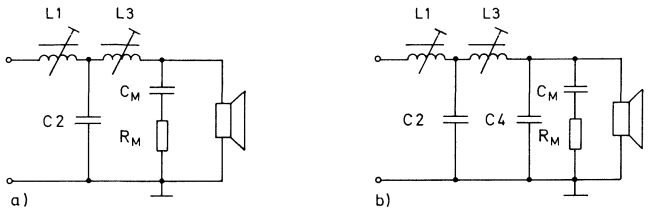


Fig. 31: Filter circuits for Class D amplifiers

3.3.6. Negative feedback

The normal method of applying negative feedback to Class D amplifiers is shown in Fig. 32. The waveform used is that at the input of the filter, i.e. a switching waveform, which is integrated by the integrator along with the audio and squarewave inputs. The reason for doing this rather than taking the feedback from the output of the filter is that the signal delay through the filter usually contributes a significant phase shift at high audio frequencies and the amplifier overall may be difficult to stabilize. However, if the feedback is taken from the output of the filter a wider variety of basic amplifier configurations becomes possible. With the high switching frequencies that are practical with VMOS transistors, this is another question that can be reconsidered.

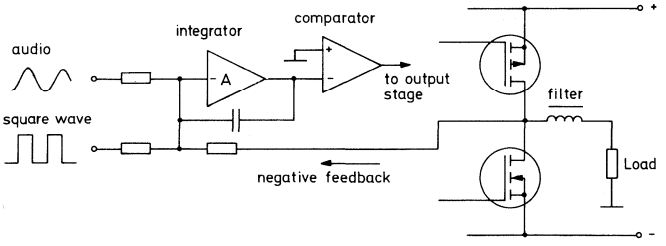


Fig. 32: Overall Class D amplifier configuration

3.3.7. Driving the output devices

To preserve the fast switching characteristics of VMOS devices the gate drive waveforms must have comparably fast transition times, otherwise the efficiency of the output stage will be degraded by power losses during the output transitions. This is a major problem, since gate capacitances are large, usually several devices will be used in parallel, and the required voltage swing is large. Ferrite beads or series gate resistors are definitely not to be used.

Fig. 33 shows VMOS driving VMOS. However, it is also feasible to use fast bipolar switching transistors as in Fig. 34. With the aid of the fast clamp diodes shown and a correctly chosen ratio of R1/R2 the bipolar devices will not saturate. The base drive of at least 2 V is obtained from a pulse transformer. Commercially available transformers will not usually have a low enough leakage inductance for this application, which requires bifilar windings or a compromise in the direction of such construction (ref. 1). A resistor between the gate and source of the VMOS output transistors is included to ensure that these are turned off in the event of the system attempting to "lock-up" in one of its two states.

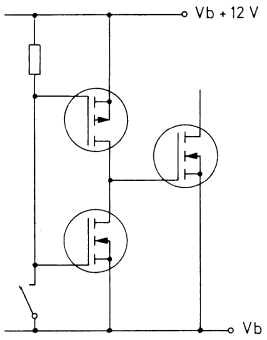


Fig. 33: VMOS driving VMOS

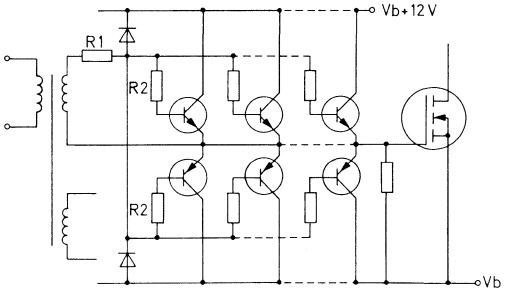


Fig. 34: Bipolar driving VMOS

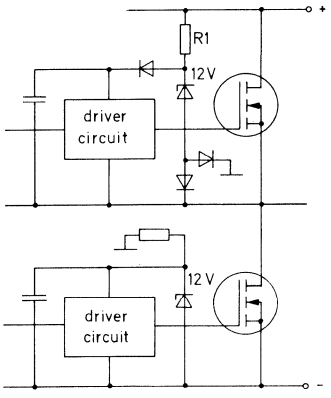


Fig. 35: Power supply for gate driver circuit

If N-channel devices are used in both halves of the output stage, some circuit like Fig. 35, which might be called digital bootstrapping, will be necessary in order to feed the gate driver circuit for the upper half. R1 needs to be dimensioned carefully, and the reservoir capacitor must be chosen on the basis of the lowest audio frequency of interest, not on the basis of f_s.

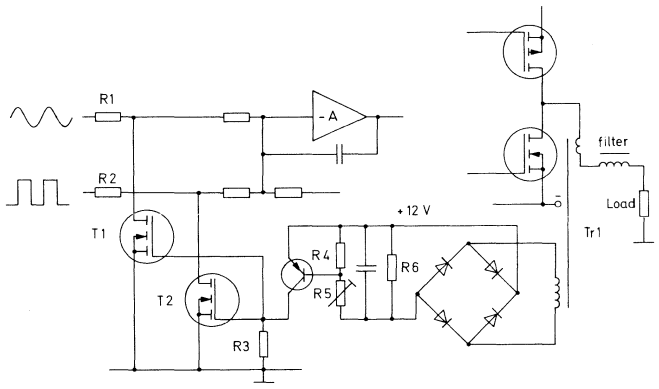


Fig. 36: Overload protection

3.3.8. Overload protection

As the output current can be sampled by a high-frequency current transformer, fast overload detection in Class D amplifiers is very easy. Fig. 36 shows a full-wave bridge – essential for accuracy – feeding load resistor R6. The output across R6 feeds a bipolar transistor via the adjustable network R4, R5. A bipolar transistor is used as it gives a sharper on/off threshold than a VMOS device, but the circuit can be redesigned so that the VMOS gates are fed directly. In practice the amplitudes of the waveforms fed into the integrator will normally be such as to demand double series switches (Fig. 43b).

Fig. 36 shows both the square-wave and the audio inputs clamped by the overload protection circuit. The advantage of this is that if R1 > R2 the operation of the overload protection system causes the audio input to be attenuated first, before the square-wave, which results in a more acceptable sound. If the current overload is due to a circuit fault, rather than to a short circuit on the output or to excessive audio drive, clamping R1 will have no effect and the clamping of the squarewave input will follow automatically.

3.3.9. Application to hi-fi amplifiers

As indicated earlier, the major consideration in hi-fi Class D amplifiers is a high ratio between f_s and f_m. Class D amplifiers are not immune to transient intermodulation distortion, as this is an artefact of the negative feedback around an amplifier. The input bandwidth limiting needed for the avoidance of t.i.m. also serves in Class D amplifiers to limit the possibility of cross-modulation products due to input signals above the audio band.

4. High frequency amplification

With their low noise characteristics, high f_T and power capability, VMOS transistors can be used at all levels from small-signal to power output, and from d.c. to VHF. R.f. circuit design is easier than with bipolar transistors because their input impedance is higher and their S-parameters are largely independent of operating levels.

4.1. Small-signal low-noise amplification

Fig. 37 shows the comparative noise characteristics of VMOS and bipolar transistors. Bipolar devices only produce good noise figures at high frequencies because they are used with low source impedances. VMOS devices produce low-noise amplification into the VHF region: e.g. a 12 dB, 20 MHz amplifier with a 2.5 dB noise figure.

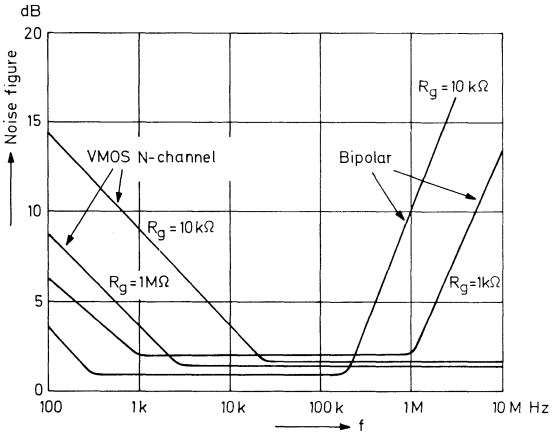


Fig. 37: Comparative noise characteristics of VMOS and bipolar transistors

4.2. Transmitter output stages

Single VMOS transistors can give power outputs of over 10 W (e.g. 12 W at 150 MHz). One particular advantage of VMOS devices, related to their freedom from second breakdown, is that they can withstand any output mismatch condition. They are thus well suited to applications such as mobile radio, Citizens' Band and radio control of models, where conditions of use are variable or unpredictable.

In addition to the usual Class A, B and C operating modes, classes D, E and F, in which the active device functions as a switch, are obvious candidates for VMOS. In classes D, E and F the theoretical efficiency is 100 %, and in practice efficiency is determined mainly by the ON resistance of the device. Fig. 38 shows the basic Class E stage (ref. 8). The choke L1 is an r.f. choke that is not involved in calculations concerning the

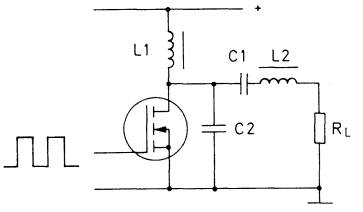


Fig. 38:
Class E output stage

frequency-determining components C1, C2, L2, R_L. The duty cycle of the waveform that drives the VMOS device is around 50 %. Fig. 39 shows the basic Class F stage (ref. 9). Again the drive waveform is about 50 % and L1 is an r.f. choke. The resonant circuit in this case consists of L2, C2. The capacitor C1 exists only to block the d.c. path from the supply voltage to the load. Another practical configuration is shown in Fig. 40.

The linear transconductance of VMOS devices makes them ideal for high-level amplitude modulation.

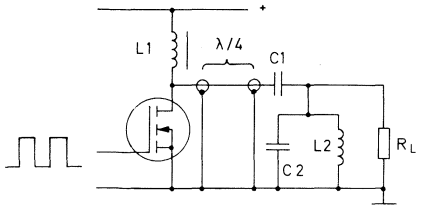


Fig. 39: Basic Class F output stage

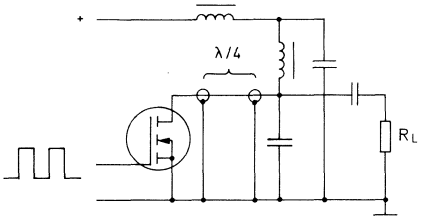


Fig. 40: Another Class F output stage

4.3. Pulse amplification

With their fast switching times, VMOS devices are ideal for pulse generator output stages. Fig. 41 shows two possible arrangements using common source and source follower circuits. In both cases there are separate controls for output amplitude (R1) and offset (R2).

Fig. 42 shows the principle of a VMOS distributed amplifier (which may also be used as an r.f. amplifier) with d.c. biasing components omitted (ref. 10). Distributed amplifiers provide useful gain, even up to frequencies where the gain of an individual active device would be less than 1, by summing the gains of the individual stages. The stages are interconnected by LC delay lines designed to give equal interstage delays in the gate circuit and the drain circuit.

The VMOS input and output capacitances by themselves may provide C_g and C_d, or they may be padded out to make C_g and C_d constant in all stages. The inductances L_g and L_d will often be low enough to be supplied by printed circuit tracks alone. The gain of a distributed amplifier of n stages is basically

$0.5 \cdot n \cdot g_m \cdot R_L$.

All stages of a VMOS distributed amplifier ca be biased together via the gate delay line, as adequate current sharing is achieved without balancing resistors.

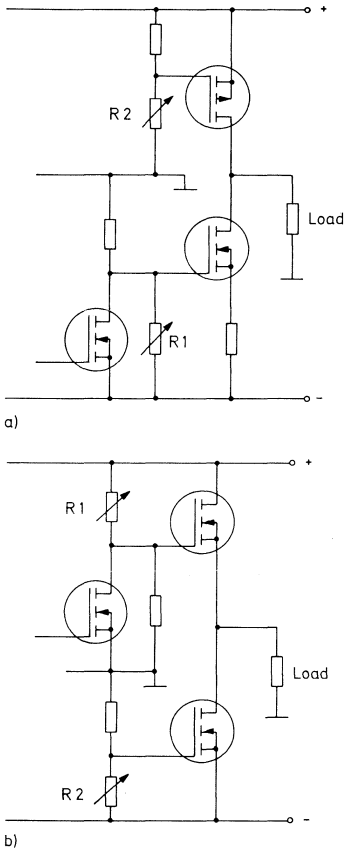


Fig. 41: Pulse generator output stages
a) Common source circuit
b) Source follower circuit

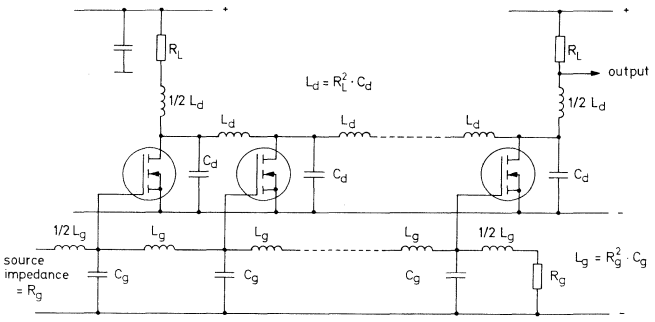


Fig. 42: Distributed amplifier

5. Analog switching and control

The low ON resistance, high OFF resistance, fast switching speeds and high degree of gate-to-switch isolation of VMOS devices make them near-ideal analog switches. With low ON resistance and rather high terminal capacitances they are particularly suited for switching from or into relatively low impedances. As their ON resistance can be varied by gate voltage and is free from any offset voltage, VMOS devices also make useful analog control elements. In the constant-current region of the output characteristics VMOS devices have another analog control application as voltage-variable current sources.

5.1. Analog switches

Fig. 43 shows the basic single and series switches using VMOS devices. All the circuit diagrams in this section are based on switching analog signals around ground potential.

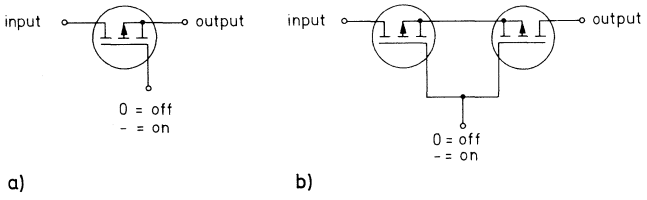


Fig. 43: Basic analog switches – single polarity
a) Single switch
b) Double series switch

In VMOS analog switches distortion of the signal has two causes. Firstly, the presence of the drain-source diode means that the resistance of the VMOS transistor when turned on is only linear up to a certain signal level. A typical V/I characteristic at a fixed gate-source voltage is given in Fig. 44 (having a "bad" diode, see section 1.). The ON resistance also becomes non-linear where the drain-source voltage passes from the constant-resistance region to the constant-current region. Secondly, the resistance of the VMOS device is modulated by the varying gate-source voltage as the voltage on the source varies about ground.

The series switch in Fig. 43b has twice the dynamic range (across the switch element) compared with Fig. 43a but also twice the ON resistance. In the complementary switches in Fig.

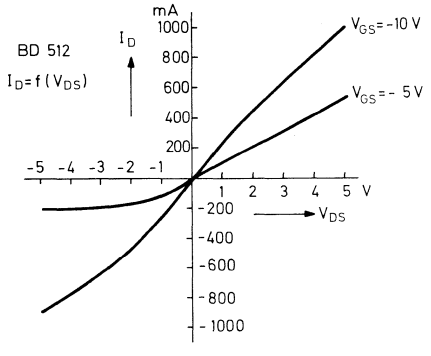


Fig. 44: V/I characteristic of VMOS BD 512

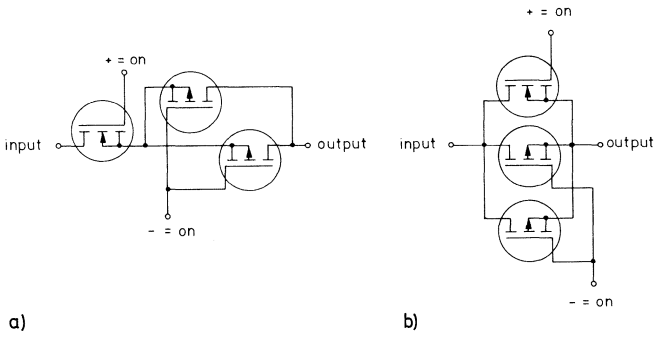


Fig. 45: Complementary analog switches
a) Series
b) Parallel

45 two P-channel devices are used in parallel because of their higher ON resistance. The circuit of Fig. 45b has the lowest ON resistance of all, but its linear region is also as small as any.

In Fig. 46, the distortion due to the varying gate-source voltage is tackled by bootstrapping the gate voltage with a Zener diode of 10...12 V. The same technique can be used with the double series switch of Fig. 43b. The signal breakthrough of any of the series switches can be improved by the Fig. 47 circuit, where the center point of the switch is taken to a suitable a.c. ground when the switch is off.

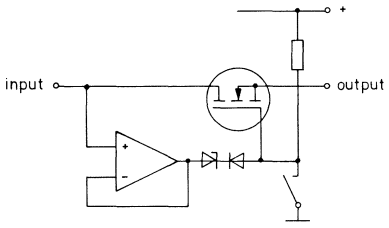


Fig. 46: Low distortion analog switch

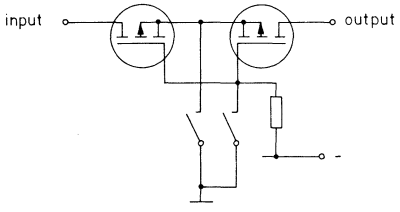


Fig. 47: Low breakthrough analog switch

5.2. Variable resistance applications

In Figs. 48 and 49, a series pair of VMOS devices is used as the amplitude control element in a Wien-bridge oscillator. The limited linear range of the ON resistance restricts the Fig. 48 circuit to about 1.5 V r.m.s. output. To overcome this restriction and to provide a 600 Ω source impedance the Fig. 49 circuit has the negative and positive feedback taken from a tap on a resistor chain driven by a current-source output stage (for which VMOS transistors are of course particularly suited).

In both circuits R1 · R2 · C1 · C2 is the frequency-determining network. A2 is a comparator, used to give amplitude control that is less dependent on frequency and temperature than the usual thermistor technique. If the oscillator is designed to operate over a wide frequency spectrum, C3 should preferably be selected according to each frequency range. In Fig. 49, R3 and R4 should be adjusted to give the desired quiescent current in the output stage. Heat sinks will be required for the output devices, but as the drains are at the same potential a common heat sink can be used, without insulating hardware.

In the resistor chain R5 should not exceed about 12 Ω. The preset resistor is provided so that the output impedance can be exactly trimmed to 600 Ω. Depending on the frequency of operation, high slew-rate operational amplifiers may be necessary for A1. High frequency compensation has not been shown on the diagrams as this will vary according to the amplifier used for A1 and the operating frequency.

At higher drain currents the transconductance of VMOS devices becomes independent of current and voltage, so that VMOS devices make useful voltage-variable power resistances. The circuit in Fig. 50 extends their range of operation to lower levels. For correct operation the two devices shown must be matched. The formula given indicates that the resistance R can be made directly proportional to V_{ref} or inversely proportional to $V_{in} - V_{ref}$. Thus multiplication and division are feasible.

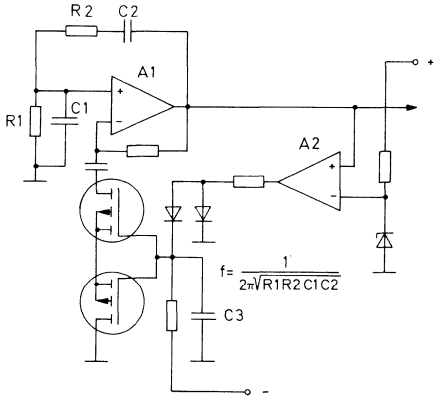


Fig. 48: Basic Wien-bridge oscillator

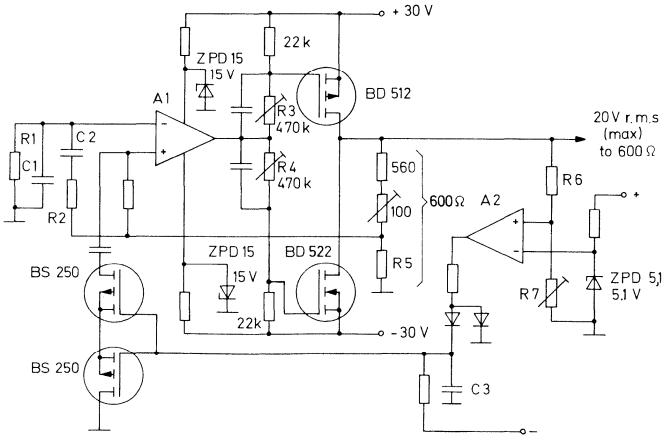


Fig. 49: High-output Wien-bridge oscillator

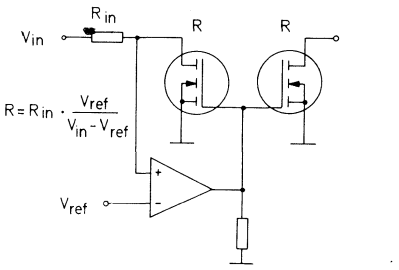


Fig. 50: Voltage controlled resistance

6. Timing circuits

VMOS transistors could have been developed specifically for timing applications. Not only are their input impedance and power gain so high that they can be connected to a circuit with a high RC time constant without unduly influencing it, but also if they directly switch a load (which is possible due to the high power gain), they do not disappear in a puff of smoke. This is because there is no such thing as forward secondary breakdown in VMOS and also because they have an appreciable ON resistance compared with bipolar transistors, so limiting the current flowing. If the ON resistance is not enough protection the output can be easily adjusted because a VMOS transistor is a wonderful current source: this is especially useful for filament lamps which have an extremely low resistance when they are cold.

6.1. Delayed turn-off circuits

6.1.1. Delay for automobile courtesy lights

Most cars (automobiles) have a courtesy light that switches on when the door is open and switches off as soon as it is closed, leaving one to fumble in the dark to insert the ignition key and put on the safety belts. Admittedly, the interior light could actually be switched on by hand, or alternatively, the door could be left open to keep the light on. Fig. 51 shows a circuit which is an "add-on" unit and will delight lovers of luxury.

When the door is open, switch S is closed, and R3 and the emitter of T2 are at 0 Volts. Thus base current will flow into T2 making currents flow in R and switching on the VMOS transistor, which supplies base current into T1.

When the door closes, switch S opens and the lamp and R3 in series become the load of T1. T2 switches off and C charges through R. Eventually the VMOS transistor passes less current, which reduces the bias on T1, increasing its collector voltage. The change in the collector voltage is fed through C, so reducing the current in the VMOS transistor still further. The effect of the positive feedback is that T1 is switched off quickly and the courtesy light goes off; the delay time is given by:

$t = 1.6 \cdot R \cdot C$

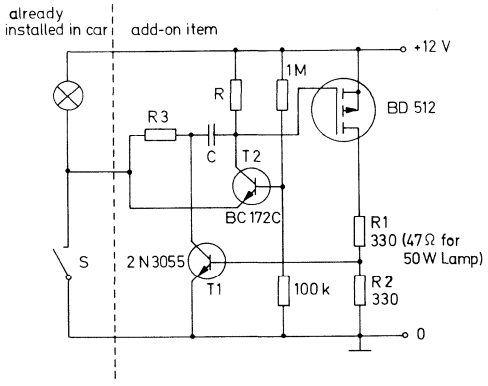


Fig. 51: Delay for automobile courtesy light

6.1.2. Turn-off delay for light

Fig. 52 is another light delay circuit, which can be used in an automobile, but it is not an "add–on" circuit; it has to be built as a complete unit. When switch S is closed, the light is switched on and current flows through diode D. The VMOS transistor is biased ON and so is the 2N3055. When switch S opens, D becomes reverse biased and capacitor C discharges only through R. Less current flows through the VMOS transistor when its gate voltage approaches the threshold voltage, so reducing the current in the 2N3055, whose collector voltage starts rising. The rise is transmitted via C to the VMOS gate and reduces the currents in both transistors further, leading to the lamp rapidly switching off. The delay time is given by:

$t = 1.6 \cdot R \cdot C$

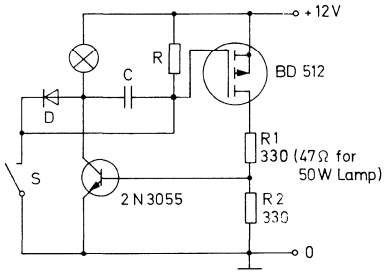


Fig. 52: Turn-off delay for light

6.1.3. Delay circuit for automobile parking lights

Fig. 53 shows a circuit which switches on the parking lights of an automobile for a certain period. This gives enough time to get out of a garage at night or have the way lit to the front door key-hole when the car is parked in the drive. The circuit can easily be added on to the electrics of an automobile without having to modify its wiring loom.

When the button is pressed, the gate of the VMOS transistor is connected to the battery voltage and at the same time C is charged up. The VMOS transistor conducts and current flows through the load, which switches the BC 327 on and hence the 2N3055, which then switches on the parking lights and also takes the other side of C up to the battery voltage of 12 V.

When the button is released, one side of C is held at 12 V and the other starts to negatively charge through R. After a certain

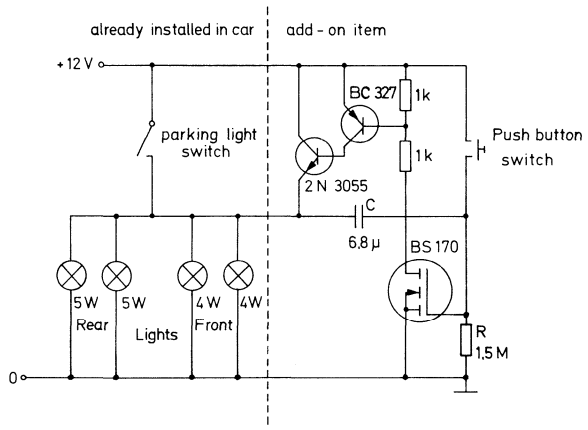


Fig. 53: Delay circuit for automobile parking lights

time, the gate voltage drops to such a level that the VMOS is no longer hard on and the current through the load falls until the BC 327 starts to cut off and hence the 2N3055 also starts to cut off. When this happens, the voltage across the parking lights starts to drop. Positive feedback via the capacitor makes the lights switch off quickly.

If C is kept at 6.8 μF, the delay time can be varied by altering R. About 1 second delay is produced for each 100 kΩ in R; thus in the circuit shown the delay time is 15 seconds.

6.2. Flasher circuit

This circuit, Fig. 54, gives a short flash with long intervals and since the current is negligible in the OFF part of the duty cycle the circuit is very suitable for battery powered equipment. The flasher can be switched on or off by connecting R5 to 0 or supply voltage.

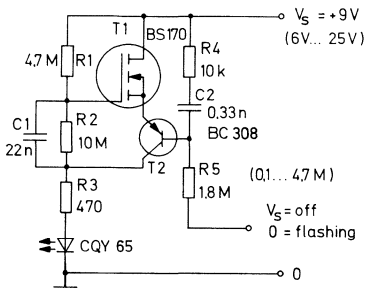


Fig. 54: Flasher

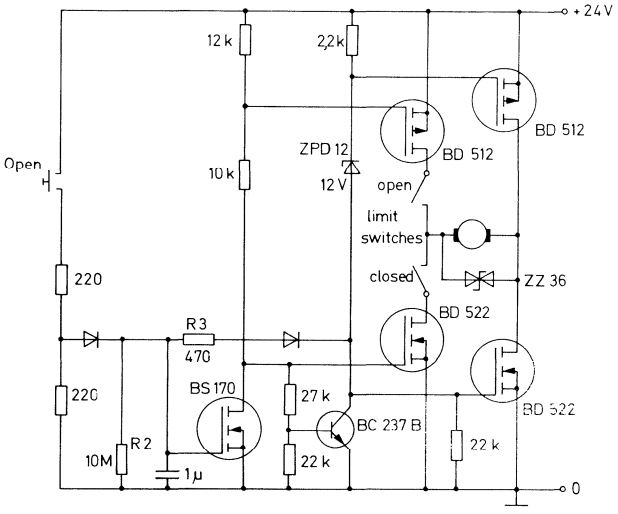


Fig. 55: Door opener/closer

When R5 is connected to the supply voltage, T2 is switched off and hence no flashing will occur. When R5 is taken to ground, C2 charges until the base of T2 gets forward biased, which causes collector current of T2 flowing through R3. The voltage drop across R3 is coupled via C1 to the gate of the VMOS transistor, making it conduct more and increasing the voltage across R3 further, which means positive feedback. In this state the LED lights and the base current needed by T2 is taken from C2. Soon a point will be reached when T2 passes less current, causing positive feedback in the opposite direction and switching the circuit off and extinguishing the LED.

The ON period of the flashing cycle is determined by R4, C2 and the base current of T2. The OFF period depends upon R5 and C2. The supply voltage also affects these times. There is a positive pulse across R3 and the LED which may serve for driving a power device if something more than an LED has to be flashed.

With 9 V supply voltage, the OFF current consumption of the circuit amounts to 0.5 μA. The pulse width of the flash is 10 ms or, if R4 is shorted, 0.4 ms. The pulse separation is about 400 ms.

6.3. Automatic door opener/closer

The circuit of Fig. 55 provides an automatic door opening/closing function as found on some trains. The circuit operates as a monostable, triggered by the "open" button. This turns on the motor to open the door. After a delay determined by the RC combination on the gate of the BS 170 (about 15 seconds here), the circuit reverts to its stable condition and turns on the motor in the opposite direction to close the door.

Limit switches are included to remove drive from the motor when the door reaches the end of its travel in either direction. To ensure good switching between the two circuit states the ratio between R2 ans R3 should be as large as possible. This avoids the possibility of the P-channel and the N-channel devices being ON together for a significant time. A bidirectional Zener diode (e.g. ZZ 36) is included to limit the voltage transient across the motor when the appropriate limit switch opens.

6.4. Timer for cooker hood

In the Fig. 56 circuit the extractor fan motor is driven at different speeds according to the resistance connected in series with it, or is driven at full speed for a fixed time. The circuit is designed for a sensitive-gate triac, which is driven in quadrants II and III. A standard-sensitivity triac may be used instead if the power supply arrangements are modified appropriately. C1 should be a tantalum type for low leakage current. The "on" time of the triac is approximately R1 · C1. This circuit is based on a suggestion by Dipl.-Ing. Wilhelm Mellewigt, Marktrodach, Germany. It may be also used for staircase lighting.

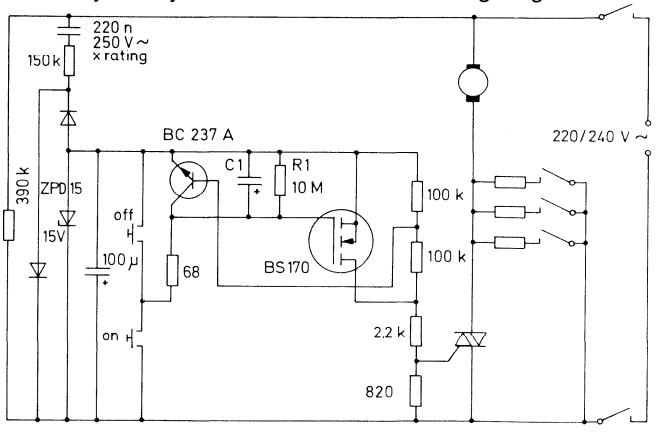


Fig. 56: Timer for cooker hood

7. Switching

In general switching applications (excluding those fields that have already been dealt with) various features of VMOS devices are significant, dependent on the particular application. The combination of high current capability (and freedom from second breakdown) with fast switching speeds represents a major advance over bipolar transistors. The low drive current and power requirements of VMOS devices permit exceptionally simple interfaces with many forms of logic. In some applications the constant-current VMOS output characteristic or the negative temperature coefficient of the output current may be important as circuit protection mechanisms, while in others the absence of an offset voltage is outstandingly useful.

7.1. Filament lamp driving

The constant-current characteristic of VMOS devices can be used to limit the inrush current of incandescent lamps, and so increase their service life. In Fig. 57a the output current is limited via the gate drive voltage. In Fig. 57b the full gate drive voltage is available but only after a delay introduced by the capacitor. The Fig. 57c circuit is particularly suitable when the ratio of inrush current to steady current is very large.

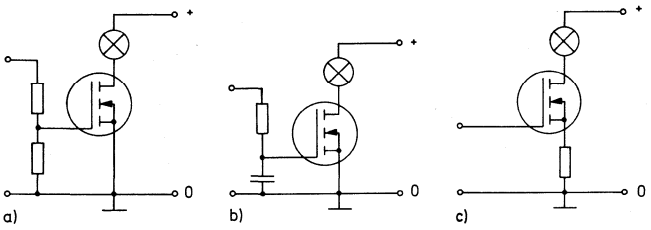


Fig. 57: Filament lamp drivers
a) Limiting via gate drive voltage
b) Limiting via delay
c) Drain current limiting by resistor

7.2. Schmitt trigger

The VMOS transistor can also be used in a Schmitt trigger circuit. An advantage is that the switch-off time is the same as the switch-on time because there is no minority carrier storage in VMOS transistors.

In the example given in Fig. 58, with 12 V supply the circuit switched over as the input rose to 4.2 V and switched in the other direction at 3.6 V. These switching levels obviously depend upon the supply voltage and the ratio between all the resistors as well as upon the production spread of the gate threshold voltage.

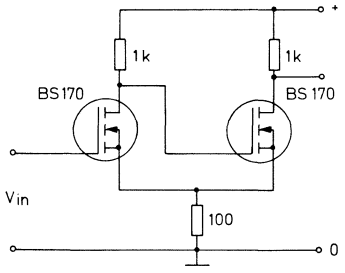


Fig. 58: Schmitt trigger

7.3. Push-button telephone

In Fig. 59 the basic configuration of a push-button telephone set is shown. T1 is the replacement for the "off/normal" contact on the telephone dial: its function is to short-circuit the transmission circuit and so to contribute the lowest possible resistance in the circuit consisting of telephone subset + line + relay in telephone exchange. T2 is the replacement for the impulsing contact on the dial.

The logic circuit only has to supply negligible power to drive the VMOS devices, which is an important benefit in electronic telephone subsets. A Zener diode is included to limit the voltages than can appear across T2 due to the inductance of the line.

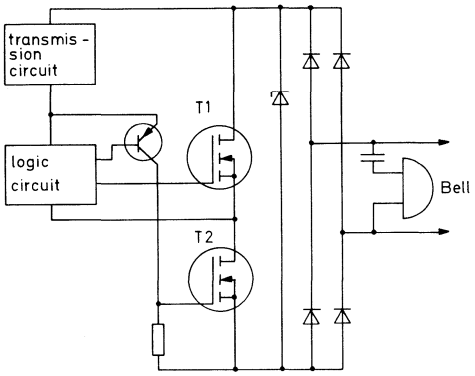


Fig. 59: Push-button impulsing telephone

7.4. Automobile ignition system

The principles behind the idea are:
– Low voltages are switched to a converter unit on each spark plug, so eliminating the distributor and long H.T. leads.
– High frequencies are used and energy is transferred, not stored, in the unit on the spark plug: the unit can therefore be small and cheap.

The principle of operation can be seen in Fig. 60.

A timing and switching unit has information on the camshaft position fed into it (to determine the time of firing and the

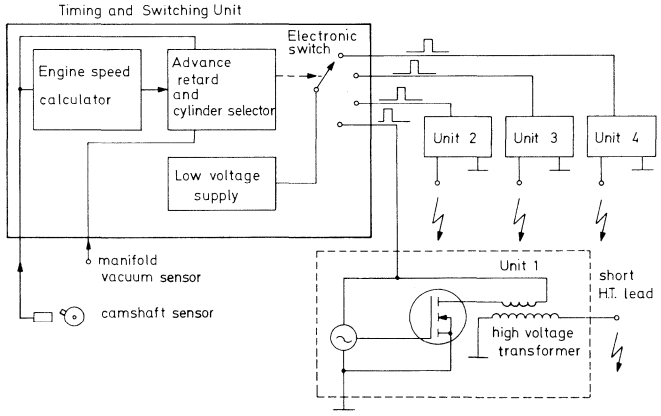


Fig. 60: Automobile ignition system

cylinder to be fired); the engine speed can also be determined from this information for advance and retard purposes. In addition a signal from the manifold vacuum is also fed in, again for advance and retard purposes. The timing and switching unit has a converter to convert the 12 V battery supply to a higher voltage and this voltage is switched at the correct moment to one of the units mounted close to the spark plugs. A duration of 1 millisecond is suggested.

The ignition unit has a high frequency oscillator of about 2 MHz using a toroidal transformer (to eliminate radiation). The oscillator circuit can be single-ended or push-pull, depending upon power and transformer requirements. The VMOS transistor(s) should operate with a squarewave output to reduce the dissipation because the ambient temperature can be very high. Since the VMOS transistor can switch in nanoseconds and has no storage time, such operation is possible. The output of the high voltage transformer (the transformer is small because of the high frequencies) goes to the spark plug.

Now let us examine what the spark plug needs. The conventional ignition system delivers about 50 mJ but there is evidence that less is needed if a high frequency is used. This 50 mJ represents a fair margin of safety because all other ignition systems have long H.T. leads and there is considerable leakage in humid conditions. As the proposed system has very short leads, the factor of safety mentioned is not needed: at an estimate, only 10 mJ are needed. By a judicious balancing of current firing times, voltage and dissipation due to the ON resistance of the VMOS transistors, 10 mJ should be possible to achieve.

Mechanical considerations would dictate that the ignition units should be mounted on a long bracket running above the spark plug positions and the units should be shielded by a reflecting heat shield to eliminate all thermal radiation possible from the engine block and spark plugs. If outside air could be ducted over the units it would be helpful.

7.5. LED driving

The VMOS transistor behaves as a current source and is hence suited as LED driver. Fig. 61 shows it driving an infrared light-emitting diode. The VMOS can be driven by TTL and the system will operate in a few nanoseconds, making it very suitable for high bit-rate transmission.

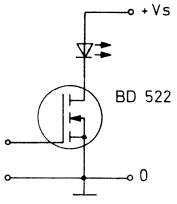


Fig. 61: Infrared diode driver

Fig. 62 is for driving visible LEDs. In contrast to IR diodes (which can handle up to 1 A) a normal visible LED has a maximum current of 50 mA. A large VMOS device does not control very linearly at these levels, so that LEDs should be connected in parallel: provided that the supply voltage is sufficient, more can be added in series as shown. Each

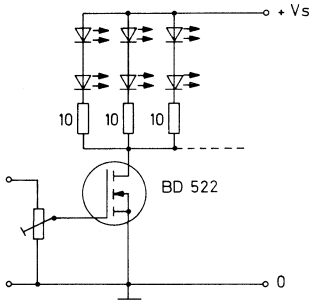


Fig. 62: LED driver

branch needs a small resistor to prevent current hogging. The brightness is controlled by the potentiometer: its top end can be connected to d.c. or to a pulsed source.

7.6. Interface with logic and microprocessors

VMOS permits the simplest possible interfaces between CMOS and power loads (Fig. 63a and b). With ECL (Fig. 64) the interface is more complex, but even so it is virtually impossible to preserve the speed of the ECL. With TTL a pull-up resistor is essential (Fig. 65), but the 5 V gate drive that results is not sufficient to drive the VMOS devices to their minimum ON resistance: for this, open-collector TTL with a pull-up resistor to +12 V is necessary. An interface between CMOS and TTL is shown in Fig. 66.

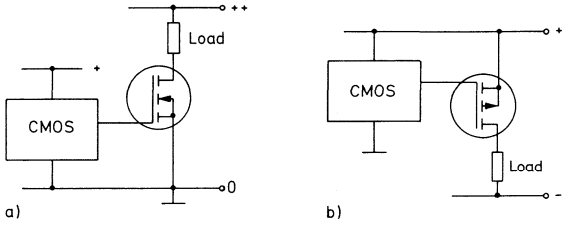


Fig. 63: Basic CMOS-VMOS interfaces
a) with n-channel VMOS
b) with p-channel VMOS

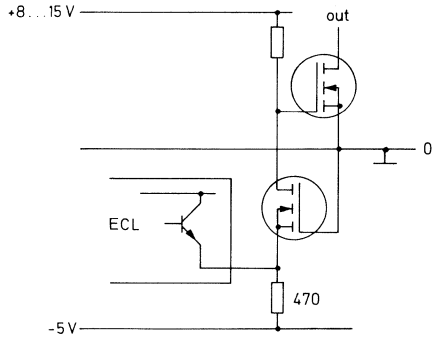


Fig. 64: ECL-VMOS interface

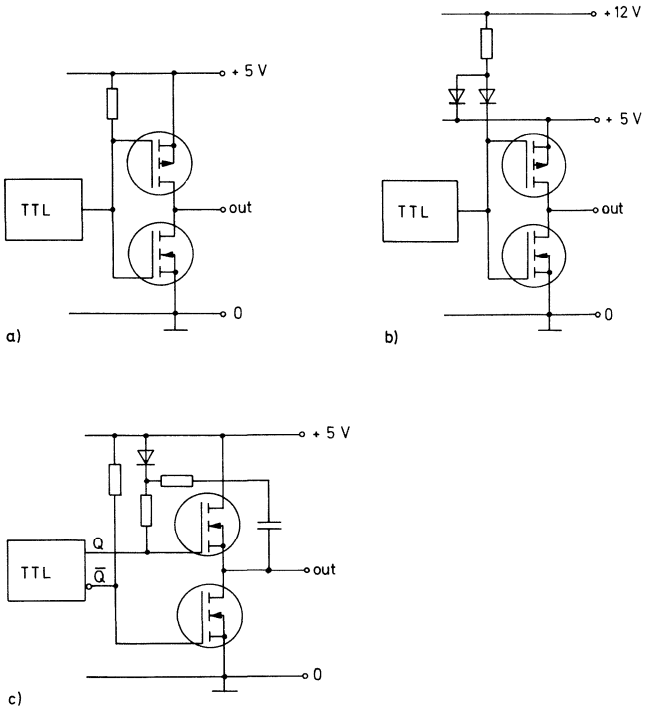


Fig. 65: Clock and memory drivers
a) Basic TTL-VMOS driver
b) with pull-up to +12 V
c) Bootstrapped non-complementary output

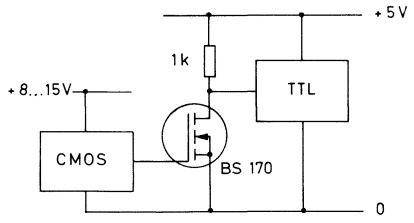


Fig. 66: CMOS-TTL interface

7.7. Clock and memory driving

For driving ferrite core and plated-wire memory arrays bipolar transistors were never very satisfactory. The requisite power handling capability (particularly as regards second breakdown limits) and the fastest switching times could not be obtained in the same transistor. With VMOS devices no compromise is necessary, as their switching speed is faster than that of bipolar transistors operating as saturating switches.

In memory driving applications, whether core, plated-wire or MOS, any improvement in the speed of the address drivers turns up as a reduction in access time. Fig. 65 shows some possibilities for driving low resistance and/or high capacitance loads such as are found in ferrite core arrays and in MOS memory cards (clock and address lines). Because of the fast rise times attainable, some resistance (perhaps 10...22 Ω) may be added in series with the output as reverse termination. Fig. 65b is an alternative to Fig. 65a that improves the fall time without demanding such a low value of pull-up resistor. Fig. 65c is practical as long as the transitions on the two TTL outputs are substantially simultaneous.

More complex drive circuits for special requirements, such as minimum undershoot on the address lines of an MOS array, are practical with VMOS because of the close relationship between drain current and gate voltage. Another bonus when driving MOS memories is that VMOS devices have no offset voltage, so that when driving capacitive loads the drive voltage actually reaches zero. This may in practice have the effect of adding a few hundred millivolts to the guaranteed noise margin of the system, compared with driving it by means of bipolar transistors or ICs.

7.8. Digital video output stage

At the present time numerous engineers are undoubtedly eyeing their portable TV sets with a view to converting them into VDUs for personal computers. Most computers can provide a modulated composite video output signal suitable for direct connection to the antenna input of the TV set, but this means that the data to be displayed passes through most of the circuitry in the set. The result is poor definition on the display due to undershoot and overshoot on the video waveform.

Many portable TV sets have a supply voltage suitable for a VMOS output stage as shown in Fig. 67 which is to be fed directly from the logic in the computer. Composite video is still to be fed to the antenna input for synchronisation purposes. The circuit shown is optimum for cathode drive, where the output is at the positive level for a blank screen, i.e. for most of the time. It can be inverted, using N-channel devices, for grid drive to the tube. D.c. biasing for control of contrast and brightness is not shown.

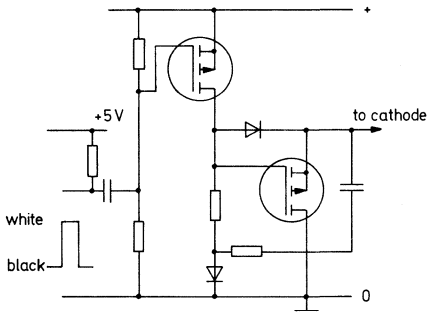


Fig. 67: Digital video output stage

8. Transducers and sensors

Most sensors only take a small amount of energy out of what they are measuring and this energy has to drive a load via an interface circuit. In the case of an electronic interface circuit, it would be ideal if it had a very high input impedance and it would be a great advantage if its power gain were almost infinite. VMOS meets these requirements to a very high degree.

8.1. Circuits for water detection

Both these circuits are for detecting water and they both rely upon the fact that water encountered in day-to-day routine is a conductor.

Fig. 68a circuit warns the car driver when the level of the water in a windscreen washer reservoir is getting low. Two electrodes dip into the water, which acts as a resistor of about 10 kΩ, putting a low voltage on the VMOS gate, and so cutting off the transistor. When there is no water, the gate voltage rises above the threshold, so causing current to flow through the single wire that leads to the LED on the dashboard. For automobiles with a positive ground use a BS 250 P-channel VMOS transistor and reverse the LED. Mechanical details are that the electrodes should be led through tubes to avoid water splashing over the seals. The main electronics should be mounted on the reservoir so that there are no leakage currents flowing between the leads to the electrodes.

The circuit in Fig. 68b warns when there is water where it is decidedly not wanted (e.g. floors of kitchens, cellars, bathrooms). The circuit is somewhat the inverse of the first: it is only when there is water across the electrodes that current flows through the buzzer. As the device should not operate often and the standby current is always negligible, this enables a battery with a long shelf life to be used and the device can be put on the floor and forgotten. A plastic box is used, with the electrodes coming out of the side and bent so that they almost touch the floor and the buzzer is mounted firmly on the outside, enabling the box to act as a sounding board.

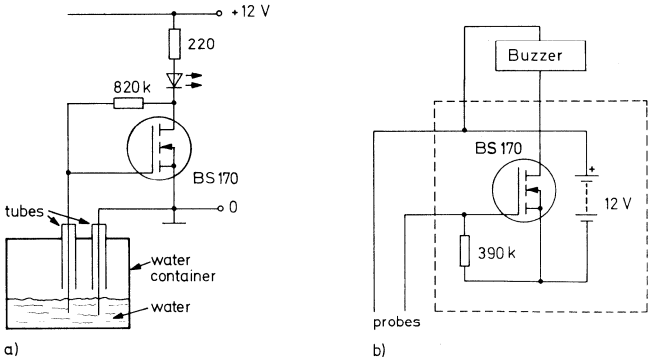


Fig. 68: Water detection circuits
a) Detection of low water level
b) Flooding detector

8.2. Touch switches

The principle of operation is that a finger capacitively or directly bridges two electrodes. The capacitive version is shown in Fig. 69a, the equivalent circuit being shown in Fig. 69b. The capacitance couples an a.c. voltage to a VMOS detector connected to the switch as in Fig. 70. Note that a 2.2 MΩ resistor acts as further protection in the case of the insulator breaking.

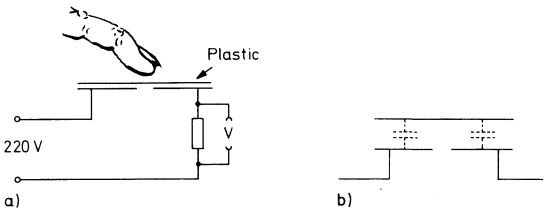


Fig. 69: Touch switch
a) Principle of operation
b) Equivalent circuit

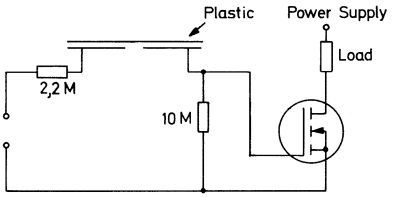


Fig. 70: Touch switch driving VMOS

Fig. 71a is a simple construction for the electrodes but the interdigitated construction in Fig. 71b makes the position of the finger less critical. In the experiment, the 50 Hz mains was used, but if a higher frequency is used, the capacitance will be relatively more effective. A finger is not essential and instead the circuit can be actuated by a piece of metal which is not connected to ground. An example could be a limit switch on a machine tool.

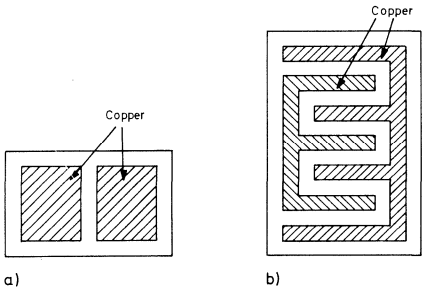


Fig. 71: Touch switch electrodes
a) Simple construction
b) Interdigitated electrodes

Two touch switches which are d.c. operated are shown in the Figs. 72 and 73. In the Fig. 72, separate touch contacts are used for ON and OFF functions. It is possible to design the circuit with a small (BS 170) and a power VMOS transistor

(BD 522) and with different load resistances in the drain circuits, e.g. 10 kΩ in the high-ohmic branch and a lamp in the low-ohmic branch. The dotted capacitors (about 1 μF) are necessary with VMOS transistors having no gate protection Zener diodes.

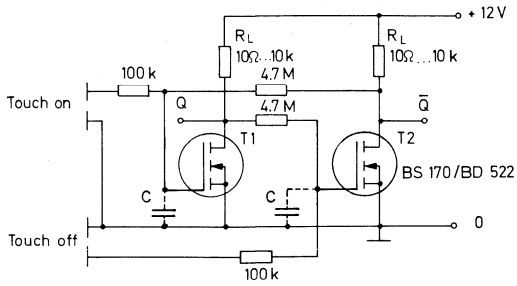


Fig. 72: Touch switch with two sensors, d.c. operated

The touch switch of Fig. 73 has only one touch contact acting for ON and OFF operation. When power is switched on, T1 will conduct, T2 is turned off and the 0.47 μF capacitor is discharged. Touching the sensor turns T2 on, and due to the 4.7 MΩ feedback resistor from drain of T2 to gate of T1 the circuit remains stable in this state. The 0.47 μF capacitor is thereby charged via the other 4.7 MΩ resistor. Touching the sensor again transfers the positive potential from the 0.47 μF capacitor to the gate of T1, thus turning it on and turning T2 off. If the sensor is touched for one second or longer, the circuit will operate as a relaxation oscillator, changing its state every second. The two load resistances may be unequal, as described at Fig. 72.

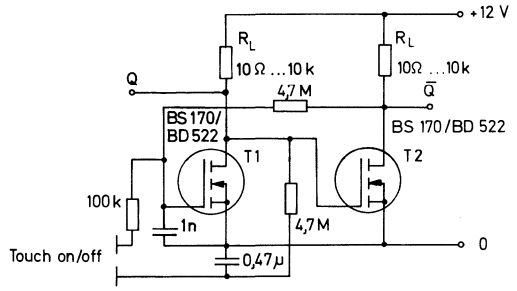


Fig. 73: Touch switch with one sensor, d.c. operated

8.3. IR audio transmitter and receiver

Advantage is taken of the linear gate voltage to drain current characteristics of a VMOS transistor and its high input resistance (in the case of the receiver). In Fig. 74, an audio signal modulates the current in the IR diode. Several diodes can be connected in series. In Fig. 75 the modulated light alters the detector current which flows through the 470 kΩ resistor, so modulating the receiver VMOS device, which directly drives headphones, or even a loudspeaker, whith no intermediate amplification. The potentiometers are to set the VMOS transistors into the linear operating region.

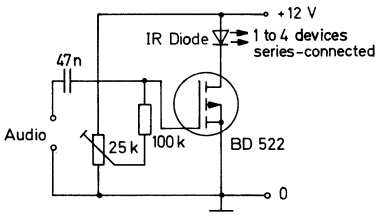


Fig. 74: Infrared audio transmitter

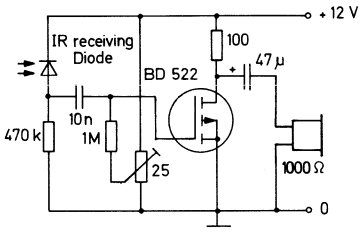


Fig. 75: Infrared audio receiver

8.4. Electronic candle

This idea is more of a party-piece, but it could also be used as an over-temperature detector. In Fig. 76 the thermistor is mounted near the filament lamp. The values are such that the light is out. When a lighted match is held near the thermistor, the VMOS transistor is biased on and the bulb lights up. The heat from the bulb is enough to keep the thermistor sufficiently heated even when the match is taken away. The light is put out by sharply blowing on the thermistor to cool it.

Fig. 76 shows the circuit in a very basic form; however, it does work satisfactorily. In Fig. 77 there is positive feedback to make sure the light switches sharply and is either fully on or fully off. The potentiometer adjusts T2 so that it is just conducting when the lamp is out.

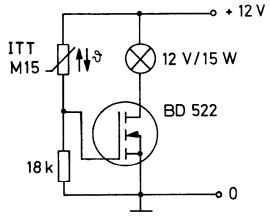


Fig. 76: Electronic candle, basic form

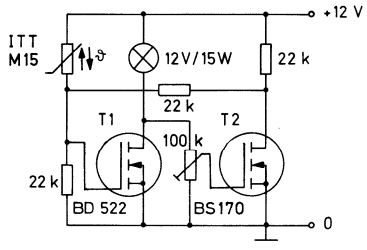


Fig. 77: Electronic candle, with positive feedback

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